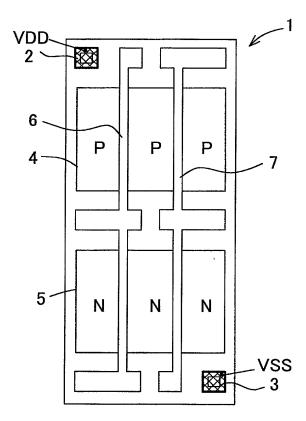
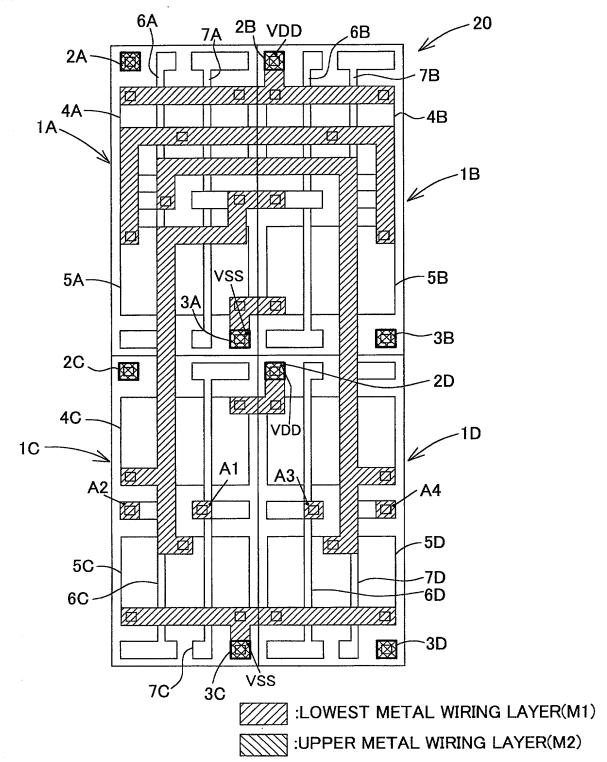
FIG. 1
FUNDAMENTAL CELL IN ACCORDANCE WITH THE PRESENT INVENTION



:LOWEST METAL WIRING LAYER(M1)

FIG. 2
FUNCTIONAL CIRCUIT BLOCK FORMED BY USING FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION

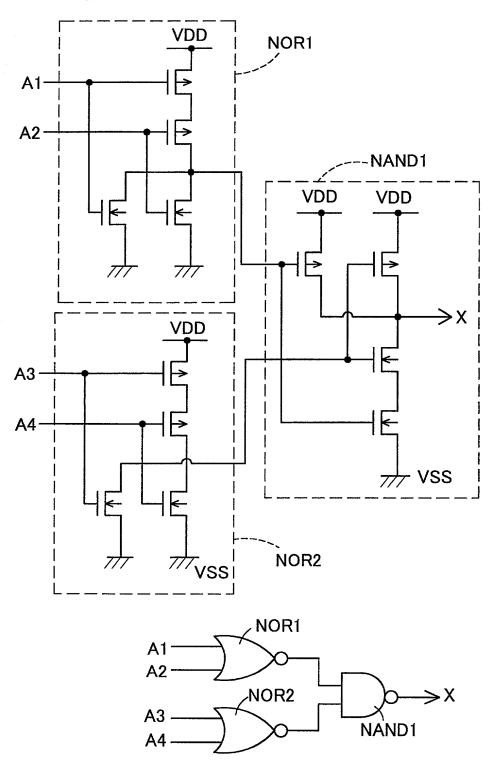


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FIG. 3
CIRCUIT DIAGRAM OF THE FUNCTIONAL CIRCUIT BLOCK SHOWN IN FIG.2



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FIG. 4

FIRST PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

							-
$\nabla\!Z$		111111111111111111111111111111111111111	ADV/////	JOK	177	MI////III	DDV 🖾
	1(1,1)	1(1,2)	1(1,3)	1(1,4)		1(1,N)	\
							☑ VSS
	101111110	Id/////		D	777	10//////01	
	1(2,1)	1(2,2)	1(2,3)	1(2,4)		1(2,N)	☑ VDD ☑ VSS
							- VOO
	•	:	:	:		:	
\square	O /////	10//////D	<u>10//////</u>		7777	W//////	ZZ VDD
	1(M,1)	1(M,2)	1(M,3)	1(M,4)	* * *	1(M,N)	⊠VSS
			7777774				27 A Q Q

FIG. 5

SECOND PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX $_{
m 32}$

														V		
	THE STATE OF THE S					3	<u> </u>				R	r				
		1(1,1)		1(1,2)			1(1,3)			1(1,4		• • •		1(1,N)		
		1(2,1)		1(2,2)			1(2,3)			1(2,4)	TITITITI		W	1(2,N)		
		•••		:			:	17777777		:				:		
/	CALLET THE THE TANK	1(M,1)		1(M,2)			l (M,3)			1(M,4	K/10/////	•••	A TITILLIA	1(M,N)		
VDD)	VSS	S VD	D /	, VI S) DE) / VS			DD '	√'S	S '	VΈ	OD	\ VSS	
JUDDED METAL WIDING LAVE																

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FIG. 6

THIRD PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

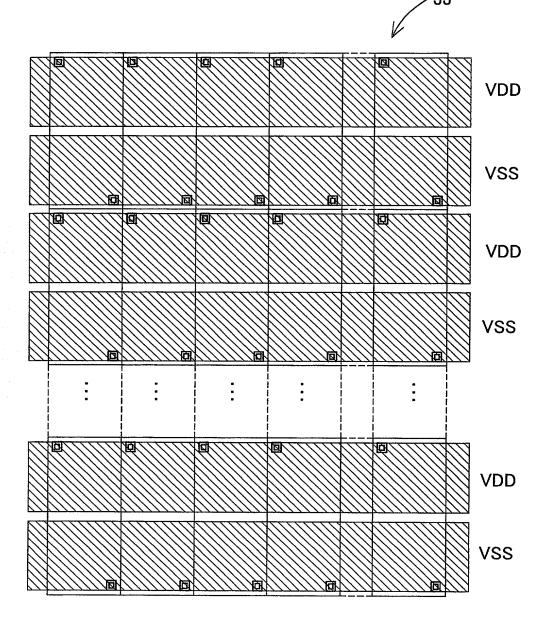
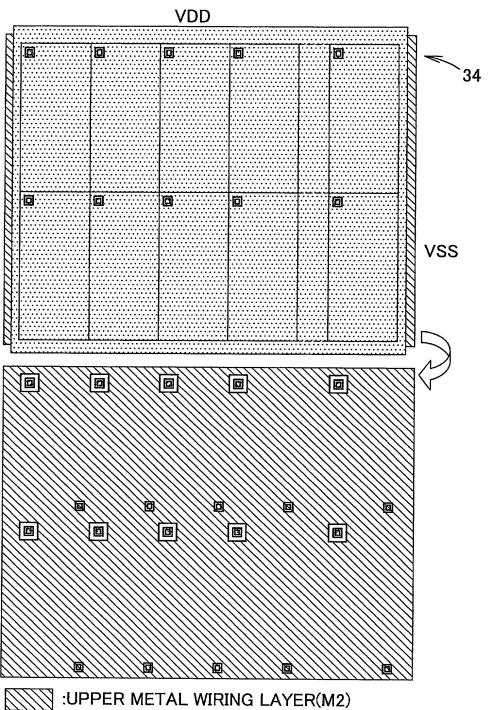


FIG. 7

FOURTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX



:UPPER METAL WIRING LAYER, WHICH IS PLACED UPWARDLY OVER THE UPPER METAL WIRING LAYER M2 (M3)

FIG. 8

FIFTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

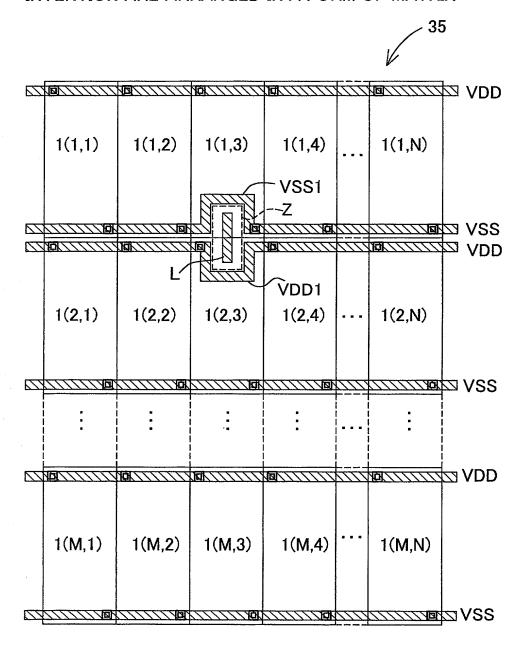


FIG. 9

SIXTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED TO FORM A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

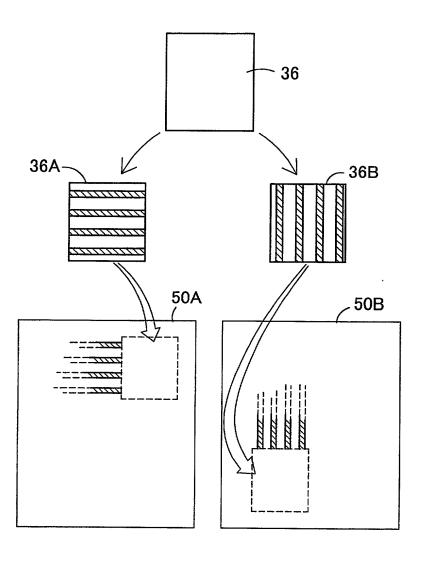


FIG. 10

BLOCK DIAGRAM OF A WIRING APPARATUS IN ACCORDANCE WITH THE PRESENT INVENTION

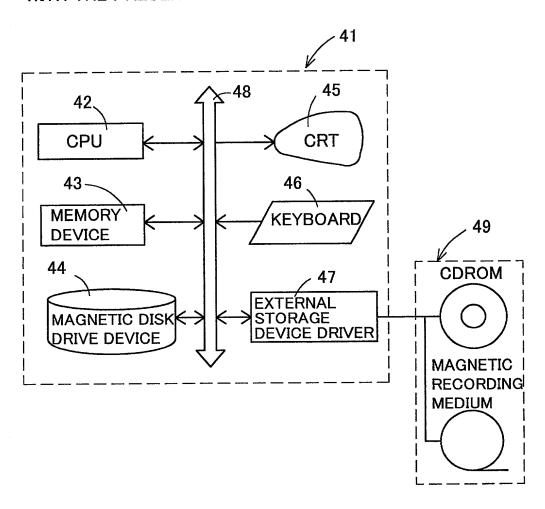


FIG. 11
A FLOW CHART OF A WIRING METHOD FOR WIRING IN A FUNCTIONAL CIRCUIT BLOCK USING THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION

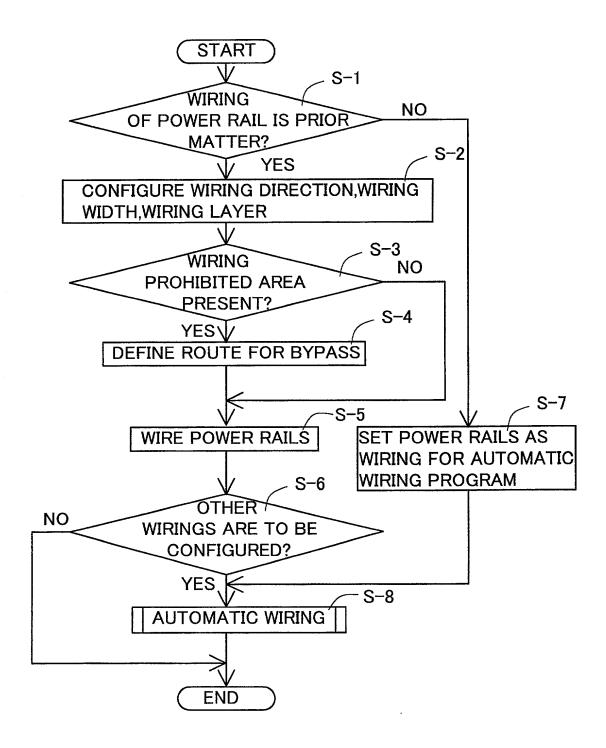
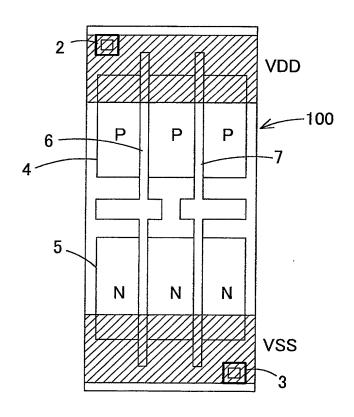


FIG. 12 PRIOR ART

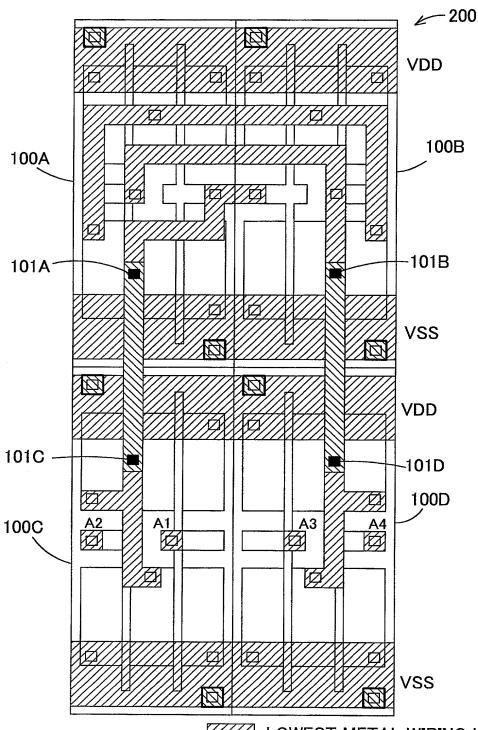
FUNDAMENTAL CELL IN ACCORDANCE WITH THE RELATED ART



:LOWEST METAL WIRING LAYER(M1)

FIG. 13 PRIOR ART

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING THE FUNDAMENTAL CELLS OF THE RELATED ART



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:LOWEST METAL WIRING LAYER(M1)
:UPPER METAL WIRING LAYER(M2)

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FIG. 14 PRIOR ART

POWER RAIL EMBODIMENT WHEN FORMING THE FUNDAMENTAL CELLS OF THE RELATED ART IN A FORM OF MATRIX

			300							
						VDD				
100(1,1)	100(1,2)	100(1,3)	100(1,4)		100(1,N)					
						vss				
						VDD				
100(2,1)	100(2,2)	100(2,3)	100(2,4)	• • •	100(2,N)					
						vss				
•	:	:	•		:					
						VDD				
100(M,1)	100(M,2)	100(M,3)	100(M,4)	•••	100(M,N)					
						vss				
		1								

:LOWEST METAL WIRING LAYER(M1)